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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,613	03/29/2004	Kyo-Min Sohn	8021-226 (SS-18859-US)	2722

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,613	SOHN ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 14-17* is/are rejected.

7)☒ Claim(s) *4-12 and 18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment received on 3/09/06. Claims 1, 2, 10, 14, 15 and 17 have been amended. Claim 13 has been canceled. Claims 1 – 21 are pending on this application. Claims 1 and 15 are independent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 3 and 14 - 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., Pub. No.: US 2005/0018521 A1 – filed Jul. 22, 2004.

Regarding independent claim 1, Figure 1 of Lee discloses a method of controlling an integrated circuit (1C) to which inputs and outputs (I/Os) are separately provided and to which a write address [WADD] and a read address [RADD] are simultaneously input during one period of a clock signal (Page 1, paragraph [0007] lines 1-3) and which comprises a plurality of memory blocks, each of memory bocks comprising a plurality of sub-memory blocks (Page 2, paragraph [0016] lines 6-7), data memory blocks corresponding to the memory blocks, and a tag memory controlling unit (Page 2, paragraph [0019]), the method comprising:

(a) receiving a write address [WADD], a read address [RADD], and write data [DIN];

(b) determining, a memory block (Fig. 3 [MB]) and a data memory block (Fig. 3 [DMB]) in which a data read operation and a data write operation are to be performed in response to the write address [WADD] and the read address [RADD];

(c) performing the data read operation or the data write operation in the data memory block according to the determination of step (b) (Page 2, paragraph [0017]); and

(d) performing the data read operation or the data write operation in the memory block according to the determination of step (b) (Page 1, paragraph [0012] lines 8-9).

Regarding dependent claim 2, Lee discloses wherein step (b) is performed by the tag memory controlling unit (Page 1, paragraphs [0013 and 0019]).

Regarding dependent claim 3, Figure 3 of Lee discloses the method of claim 1, wherein step (d) further comprises:

(d1) when the data read [R_DATA1] operation is performed, transmitting the read data [R_DATA1] to a transmitting unit [300] corresponding to a sub-memory block [SMB] inside the memory block [MB];

(d2) transmitting the data transmitted to an output buffer [Q0, Q2, Q3]; and (d3) outputting the data transmitted to the output buffer [DOUT].

Regarding dependent claim 14, Fig. 3 of Lee discloses the method of claim 1, wherein the tag memory controlling unit (Page 1, paragraphs [0013 and 0019]) to the

memory blocks [MB] or reads data from memory blocks [DMB] in response to the write address [WADD] or the read address [RADD].

Regarding independent claim 15, Figures 3 of Lee discloses a method for performing a write operation and a read operation in an integrated circuit (IC) [300] comprising a separate input and output (I/O), a plurality of memory blocks [MB], each of the memory blocks comprising a plurality of sub-memory blocks [SMB], data memory blocks [DMB] corresponding to the memory blocks [MB], and a memory controlling unit (Page 1, paragraph [0013] lines 7-8), the method comprising:

receiving a write address (Fig. 1 [WADD]), a read address (Fig. 1 [RADD]) and a write data command [A0, A2, A4, A6] during a period of a clock signal (Page 1, paragraph [0007]);

determining, a first memory location [MB] and a second memory location [DMB], where a write operation and a read operation are to be performed in response to the write address (Fig. 1 [WADD]) and the read address (Fig. 1 [RADD]); and

performing the write operation in one of the first memory location [MB] and the second memory location [DMB] and the read operation in one of the first memory location [MB] and the second memory location [DMB] (Page 2, paragraph [0017]).

Regarding dependent claim 16, Fig. 3 of Lee discloses wherein the first memory location is a memory block [MB] and the second memory location is a data memory block [DMB].

Regarding dependent claim 17, Fig. 3 of Lee discloses wherein the determination step is performed by the memory controlling unit (Page 1, paragraphs [0013 and 0019]).

Allowable Subject Matter

3. Claims 4 - 12 and 18 - 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4, the combination as claimed wherein at least the limitation of "wherein steps (a) through (d) each represent a stage of a pipeline in a pipeline structure in which an operation of the IC is performed".

With respect to claim 10, the combination as claimed wherein at least the limitation of "step (d) further comprises: performing a data read operation in a sub-memory block corresponding to the read address; and writing the read data to a sub-memory block in which data read in step (c1) is stored" is not disclosed, suggest, or rendered obvious by the prior art of record.

With respect to claim 18, the combination as claimed wherein at least the limitation of "determining if data stored in one of the first memory location and the second memory location is valid data" is not disclosed, suggest, or rendered obvious by the prior art of record.

Dependent claims 5 – 9, 11– 12 and 19 – 21 are allowed based on the allowance of the respective independent claims 1 and 15 above.

Response to Arguments

4. Applicant's arguments filed 3/9/06 with respect to claims 1 - 21 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

5. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is 571-273-8300

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 5/2/2006

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800